Phase-Shift DC-DC Converters' Digital Control, Control Hardware in the Loop and Hardware Real Time Simulation Study

Brian Mohsen Mirtalebi
PHASE-SHIFT DC-DC CONVERTERS’ DIGITAL CONTROL, CONTROL HARDWARE IN
THE LOOP AND HARDWARE REAL TIME SIMULATION STUDY

By

BRIAN MOHSEN MIRTALEBI

A Thesis submitted to the
Department of Electrical and Computer Engineering
in partial fulfillment of the
requirements for the degree of
Master of Science

Degree Awarded:
Spring Semester, 2012
Brian Mohsen Mirtalebi defended this thesis on March 30, 2012.

The members of the supervisory committee were:

Hui Li
Professor Directing Thesis

Petru Andrei
Committee Member

Uwe H. Meyer-Baese
Committee Member

The Graduate School has verified and approved the above-named committee members, and certifies that the thesis has been approved in accordance with university requirements.
To my mother who ignites and my son who drives my inspirations.
ACKNOWLEDGEMENTS

The author should take the opportunity to thank the Department of Electrical and Computer Engineering at Florida State University especially my defense committee, Dr. Hui Li, Dr. Andrei Petru, and Dr. Uwe Meyer-Baese for their persistent support. In addition the author must add that, this project wouldn’t be possible without the mentorship and leadership that Dr. Li throughout the life of this project has provided me. Dr. Petru had a key role in guiding me with respect to finding an appropriate numerical solution to the system of differential equations. The author has had enlightening discussions on FPGA and DSP technologies with Dr. Meyer-Baese.

My special thanks goes to my colleagues at Center for Advanced Power Systems (CAPS), Dr. Li, my mentor and advisor, for providing me with all the materials that the author needed for this project in addition to mental guidance and preparedness, Dr. Streuer for real time simulation applications, Mr. Solderbeck for RTDS interfacing and familiarizations and also all the members of Dr. Li’s team for, brainstorming, troubleshooting, and providing me with additional materials that significantly reduced the time to achieve all these.

In addition the author should thank FSU-FAMU Electrical and Computer Engineering administrators, Dr. Foo, the ECE department chair, for his leadership and support, Mrs. Natalie Sweesher for help on many fronts especially last-minute administrative and schedule issues and Eric Sapronetti for support on my TA and RA paperwork. I reserve the last sentence of this paragraph for two years of constant support and kindness, and general guidance from Mrs. Melissa Jackson.

Thoughts of the author’s son has been the main engine to efforts and also his mother has always encouraged him to pursue higher education and be a useful member of the society, his father taught him to stay the course and not losing sight of what it comes next. They are in his heart always and there are no words which can nearly express his feelings and appreciations for them.
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ABSTRACT

Having about nine years of industry experience the author clearly appreciate the results that a model-based design can bring about. The backbone of simulation is nothing but mathematical equations from simple linearization method to solving complex differential equations. Although simulating a real system with realistic outcomes is a hard task to come by but minimizing the amount of rework required after design makes it a very desirable method to see results before building a device.

The scope of this thesis paper is to bring to the light the concept of simulating power electronics devices purely in form of equations to reduce the cost of development, to speed up the time to market of the product and to establish design benchmarks to guide the designer to the right direction.

The thesis topic started as a simple application of converting an analog-based control of DC-DC converter to a DSP-based digital control, but it quickly developed into control hardware in the loop project. This shows how powerful and effective a DSP-based simulation can perform. This and a demand from the application engineering perspective made ignited the main motivation to explore different methods that can be even more effective.

After some research around the idea, it came to light that there has been some work done in the past but nothing to the effect of utilizing a DSP to simulate DC-DC converters. Therefore the last part of this thesis is to study feasibility of utilizing DSP as a real time simulator of power electronics devices especially high frequency DC-DC converters.

Although the results on the last part of the project are not definitive but there are very strong signs showing that in the future there is very strong potential of DSP-based real time simulation for power electronics devices.

This along other advantages that real time simulation can bring about such as, speed of simulation in opposed to a slow, off-line, and computer-based simulation, significant cost reduction, portability, and creating a guided-design are a few advantages to name.
CHAPTER ONE

INTRODUCTION

1.1 Research Background

As the smart grid concept grows the real time simulators of power systems include more devices in their topologies to represent a better resemblance of the real world. One of the major components in smart grid is a DC-DC device. DC-DC devices are the main component in Solid State Transformers (SST). A smart grid topology can employ usually several SSTs devices. Building the actual hardware is expensive, time consuming and difficult to simultaneously interface with the simulator. Figure 1.1 illustrates the position of the SST devices in a typical power system topology. As it is shown various SST devices can be utilized in a smart grid and building the hardware for all of these devices can be time consuming with a high price tag.

Figure 1.1: Typical topologies of a power network as SST devices are an integral part of.
1.1.1 Hardware Configuration of Solid State Transformer

STT comprises of three parts: high voltage and medium frequency rectifier, high and low voltage and high Frequency DC-DC converter, and finally low voltage low frequency inverter. As it is shown in the Figure 1.2 in a SST device the DC-DC converter links the rectifier to the inverter. [6]

![Figure 1.2: Solid State Transformer Hardware Configuration](image)

1.1.2 Software Implementation of DC-DC Converter Control

Since the DC-DC converter is the high frequency and an important part that not only translates the voltage level but also regulate it, therefore the control algorithm of the DC-DC converter utilizes a unique form. The control algorithm is composed to somehow to reduce the switching noise on the rail and also to target a higher efficiency from its predecessor topologies. [14]

1.1.3 Study of Real Time Simulation of DC-DC converters

As the DC-DC hardware topologies are utilizing faster switching frequencies, more complex hardware topologies, and complex control algorithms, there has been an increasing demand for computer-aided simulation that facilitates the research tasks, reduces the cost of
development and shortens the-time-to-market of the concept. As there has been many off-line simulation available through utilizing off-the-shelf software such as Matlab®.

Simulation results in cost and time saving because it allows easy confirmation of prototype, precise design and prediction of design errors in an early stage. Some significant problems are frequently encountered in power conversion circuits and system simulations such as: [17] [18]

- Inefficient simulation time occurs due to presence of a large number of high frequency power switching devices.
- Non-linear switching operation, complicated states and circuit modes are hard to simulate in real time.
- Convergence problem becomes prominent if power switching device models with complicated parameter settings are used.
- In case of digital circuit simulation, modeling and analysis of its related digital control scheme is difficult.

1.1.4 Power System Real Time Simulators and DC-DC converters

The power system simulators are optimized to simulate large-scale devices with low process speed in Hz range but some DC-DC devices operate in kHz range, making it impossible to simulate these devices in the power system simulators.

Center for Advanced Power System (CAPS) uses a state-of-the-art simulator called RTDS® for simulating power systems. Its smallest time step (resolution) is greater than 2 microseconds. However in a typical switching period of 20 microseconds the minimum and maximum phase-shift fluctuates from 0 to 45 degree. This translates to 0 to 3 microseconds time span. So the resolution provided by RTDS is practically useless to let us properly control a bi-directional DC-DC converter.
CHAPTER TWO

STATE OF THE ART

This chapter summarizes the work that has been done, the accomplishments of this research, and also the challenges this project has been faced to with respect to digital control of, Control Hardware In the Loop, and the real time simulation of DC-DC converter.

2.1 Digital Control of a DC-DC Converter

There has been many works done on digital control of DC-DC converters especially the Bi-directional type. However previously the utilization of fast DSP’s has been limited due to complexity of programming [1] and also large scale hardware development. [9]

![Figure 2.1: Shows the existing analog controller.](image)

The Spectrum Digital EZ DSP TMS320F28335 evaluation board with TI chip TMS320F28335, a floating point microcontroller, was utilized. It has 150 MIPS that comparatively can run as fast as 1 GHz microprocessor considering pipelining of 8 instructions per cycle. The mentioned DSP was utilized for open and closed loop control scheme that will be explained in much detail in proceeding chapters. Developing the digital control algorithm helped...
to develop a deep understanding of DC-DC converter’s circuitry that laid the foundation for the next tasks in this project.

2.2 Control Hardware In the Loop (CHIL) of DC-DC Converter

Although the concept of control hardware in the loop been around for a while but there has never been any work done on bi-directional Dual H-Bridge (DHB) DC-DC converters. A method was started to interface the control hardware circuitry of DSP with a real time simulator, RTDS®. The most challenging part of this section of the project was to interface DSP circuitry with the RTDS. The details of the work done will follow soon in the next chapters. [7]

2.3 Study of Real time simulation of DC-DC Converter Using State-Space Equations

During performing the CHIL project it was realized there are limitations to RTDS simulations. Although the RTDS simulator was able to successfully simulate the low frequency components of the SST device, which included the rectifier and inverter parts but it failed to fully perform simulating the high frequency switching functions. The previous work on simulating these parts has been successful except the entire simulation has failed due to high frequency parts, which is the DC-DC converter part. Figure 2.1 and figure 2.2 show the illustrates the circuit diagram of a multi-module DC-DC converter before and after that utilizes the mentioned DSP board respectively to receive the reference value, perform control algorithm and output the appropriate PWM signals with the right sequences that includes a suitable phase-shift value for each PWM channel.
Since the RTDS is designed for large power systems, it has a very limited number of switch components available in the small time step environment that are modeled after RLC circuits. A MOSFET device that is often used in DC-DC converters is simply not available in small time step environment. On the other hand, RTDS gives only component building capabilities in the large time step environment which has an even worse resolution around 50 microseconds. Therefore, the current simulator is not able to accommodate the new generation of the DC-DC converters.

The RTDS simulator is able to successfully simulate the low frequency components of the SST devices. This includes the rectifier and inverter parts. There are previous works on simulating these parts that have been successful except the entire simulation has failed due to high

Figure 2.2: Conversion of analog control circuit to digital for three cascaded dc-dc converters.
frequency parts which is the DC-DC converter part. The best real time simulators available in the market cannot cope with this trend.

The control hardware in the loop test was performed with PI controller and the real time simulation greatly degrades for switching frequencies greater than 2kHz. The plan was consulted with various personnel familiar with RTDS operation and also reviewed RTDS’ released documents. RTDS is not capable of simulating high frequency power devices. Since the RTDS is design for large power systems, it has a very limited number of switch components available in the small time step environment that are modeled after RLC circuits. A MOSFET device that is often used in DC-DC converters is simply not available in small time step environment.

RTDS gives only component building capabilities in the large time step environment, which has even a worse resolution around 50 microseconds. Therefore the current simulator is not able to accommodate the new generation of the DC-DC converters. The trend of new DC-DC designs is increasingly going towards switching with higher frequencies. A dual half bridge DC-DC converter that is used in a solid-state transformer topology normally operates in about 50 kHz switching frequency. [10]

The only solution appears to be useful is to utilize external simulators that can mimic an actual device to the RTDS. There has never been done modeling a bi-directional DC-DC converter in a DSP utilizing state-space equations and C language. There are two platforms that are normally used for similar ideas such as, DSPs/ high-speed microcontrollers, High speed FPGAs.

On the other hand, FPGA interfacing with RTDS is much more complex requiring developing unique and proprietary communication protocol that will yield to a longer developmental process. FPGAs use an uncommon language such as hardware descriptive language (HDL) where DSPs use common C language, which are much easier to understand, compile, debug and maintain.

Although in previous works, there have been attempts to model a DC-DC converter’s average model but there has never been any work or study done on the switching model of a DC-DC converter before. [8] [11] [12] [13] [19] [22]

In the paper under the title, “model based design of regulated bi-directional DC to DC converter” by G. Themozhi et al a converter has been modeled in Matlab® and then an additional software called DSP builder® has been used to convert and download the Matlab
codes into Altera FPGA. Please note, Figure 2.3 depicts how the DSP Builder converts a program composed in a graphical fashion to a text-based program. [3]

![Graphical Programming](image1.png) ![Textual Programming](image2.png)

Figure 2.3: How to utilizing DSP Builder® software to convert Simulink® to HDL codes.

However using the method illustrated in the figure 2.3 has the following disadvantages, as it adds extra developmental costs for utilizing costly software. The code passing through independent packages create software overhead that can make the code non-transparent, inefficient and in many cases slow resulting in unrealistic model.

On the other hand, the advantage of utilizing Matlab model is that the code can be generated automatically and quickly on FPGA platform however it requires additional efforts to interface the FPGA with RTDS.

In the paper under the title, “simulation of series-parallel resonant DC-DC converter system with DSP based digital control scheme for medical x-ray use”, by S. Mobin et al, a relatively more complex DC-DC converter has been simulated on an actual DSP utilizing state-space equations through matrix operations. [4] [20] [21]

The advantages to this method are as follow, utilizing C language, transparent and maintainable coding practices, producing optimized and hard real time codes, inexpensive developmental process.

However the disadvantages to this solution are, that the challenges mentioned earlier pose a tedious task of design and development through mathematical modeling which in turn translate
to a longer code developing process. However the RTDS interfacing is much simpler compare to FPGA platform. Also this model does not represent the Dual Half Bridge DC-DC converter.

Modeling a bi-directional DC-DC converter on DSP considering its switching dynamics has never been done. The model can offer a real time simulation to the RTDS system with minimum interfacing complexity that has never been done. Cloning the DC-DC model is the least expensive compared to FPGA platform which utilizing this tool has never been done. [7] [13] [15] [16]
As it was mentioned in the previous chapter, there has been some previous works in the area of converting analog control mechanism to digital control. However performing this task helped familiarizing with the concept of digital control of the DC-DC converters. [1]

It was advised an advanced DC-DC converter topology to be studied thoroughly in order to design the control scheme. This was because this topology was already developed as hardware and there was tremendous amount of expertise around it to direct this research project to the right direction. As a result a current-fed zero voltage switching (ZVS) bi-directional Dual H-Bridge (DHB) DC-DC converter topology was examined. [2]

As it was mentioned in [2] there were thirteen steps required in order to construct the control signals for four switches. The following picture illustrates the initial construction of the control signals. Figure 3.1 illustrates the PWM pattern required for a phase-shift control scheme.

Fig 3.1: Switches’ gate signals and sequences
To calculate the $\phi$’s values the power is calculated. The scope of utilizing power calculation is to maximize the efficiency of the device hence:

$$P_o = \frac{V_{in}^2}{\omega L_s} \cdot \frac{\phi_i (\pi - \phi_s)}{\pi}$$  \hspace{1cm} (3.1)

$$D = \frac{\phi_s}{2\pi}$$  \hspace{1cm} (3.2)

In equation 3.1, $P_o$ is the output power in Watts, $V_{in}$ is input voltage in Volts, $\omega$ is switching frequency in Radian/Sec, $\phi_i$ is the phase shift in Radian, $L_s$ is leakage inductor’s inductance for the primary-referred model in figure 3.2. In the equation 3.2, $D$ is the duty cycle. Since the duty cycle won’t have a significant effect on output power a duty cycle of 50% will lead to a $\phi_2 = \pi$. In figure 3.2 the four switches are controlled with the four PWM signals in figure 3.2.

![Current-fed bridge and Voltage-fed bridge](image)

Figure 3.2: Current-fed primary-referred dc-dc converter. [2]

At the start of the project it was decided to compose the code for only open loop control of the switching signals in order to establish correct switching sequences. Figure 3.3 illustrates the open loop algorithm of the open loop control.
As the initial open loop control was set up, the research moved on to implementing the closed loop control based on the following closed loop diagram. The Vref sets the voltage reference and DSP receives the set voltage through the ADC channel. Then signal is being regulated through the proportional and integral controller generating appropriate PWM signals. Finally the sensor monitors the output voltage and reports back the well being of it. Please note figure 3.4.

In figure 3.5 the closed loop program algorithm is illustrated through a program flowchart. The process is similar to what was explained for the closed loop control diagram mentioned in the last paragraph.

Figure 3.3: the open loop control of the switching
Figure 3.4: Closed loop control diagram.

Figure 3.5 illustrates the programming flowchart that was implemented in ANSI C language on DSP platform.

Figure 3.5: Programming flow chart for the closed loop control algorithm.
There are several characteristics to DHB dc-dc converter that the TI DSP was able to successfully employ. The phase shift for controlling the power and the dead band controller for the soft switching as well as frequency and duty cycle of the PWM signals, all were accessible through special registers on the DSP. The TI DSP ePWM module is able to handle both phase-shift and dead-band conditions through specific registers and allow the controller algorithm to access them on the fly without interrupting or delaying the control algorithm. Please note figure 3.6 for further information.

![Diagram of Signal sequences considering the TI DSP special registers](image)

**Figure 3.6: Signal sequences considering the TI DSP special registers**

In figure 3.6 the dynamics of PWM pattern generation is explained in conjunction with the DSP special registers designated for the same purpose. Also as it is shown in figure 3.7, the PWM construction is via programming a timer and setting a compare register value. In this case for a symmetrical PWM signal a count-up and down scheme was used.
Figure 3.7: DSP internal registers to construct the PWM signal for each PWM channel.
CHAPTER FOUR

CONTROL HARDWARE IN THE LOOP (CHIL) OF DC-DC CONVERTER

Since RTDS real time power system simulator was not able to simulate high frequency switching function of dc-dc converter it was decided to implement control hardware in the loop scheme to examine the limitations of the real time simulator. The followings are the result of that study.

Figure 4.1: DC-DC converter model that was built in small time step RTDS environment.
As it is shown in figure 4.1, a phase-shift dc-dc converter was built in RTDS small step environment. The figure is just to illustrate how similar the small step environment is with some familiar SPICE software packages.

There are two real time environment available in RTDS named large and small time step environments. The large time step environment provides the designer with various components from its library to emulate power system devices. Unfortunately due to the new topology of solid-state transformer particularly with respect to its high frequency dc-dc converter the large time step components were not compatible with the solid-state transformer technology. The large time step real time simulation utilizes components that must be have a processing time of at least 50 microseconds. The switching time in a typical dc-dc converter is about 20 microseconds therefore modeling the converter in large time step environment was out of the question.

On the other hand the small time step environment that was as fast as 2 microseconds time intervals could not provide the dc-dc model with right switches or dc-dc topology. However it was decided to try it out and document the limitations. So it was planned to provide the control signals to the gates of the switches with DSP and have the model to output the model’s output voltage through its analog output to the analog to digital input of the DSP board.

![RTDS -DSP interfacing configuration](image)

Figure 4.2: RTDS –DSP interfacing configuration
To interface the control signal with the RTDS’ input there were some limitations as the RTDS needed at least a 5mA current for each PWM channel in order to be able to receive the signal through a long cable that would connect all four channels of the DSP’s PWM signals to digital I/O card of RTDS. Figure 4.2 illustrates this connectivity process. An open collector BJT switch was used to convert the output voltage of 3.3 volts and a few hundreds of microampere to voltage and current level that was acceptable for the RTDS’ input, 5 volts with about 5 miliamperes.

To supply 5mA current for each channel an extra power supply was utilized that would channel and switch the appropriate voltage and current via open collector configuration of a BJT. The GTDI is a general-purpose digital I/O card that RTDS uses to receive digital signals as an input. The input voltage to the BJT was 3.3 volts with a few hundred of uA current and the output was 5 volts with 10 mA.

Figure 4.3 shows the DSP interface board with BJTs. To the right of the picture there is the DSP evaluation board and to the right the prototype of BJT banks. Figure 4.4 illustrates the RTDS digital I/O connection with the cables routing the control signals from DSP.

Figure 4.3: DSP interface board and DSP board.
Prior to running the closed loop real time simulation of the dc-dc model in RTDS, the open loop control was ran in order to verify the integrity of the signals and interfacing model. Figure 4.4 shows the result of what DSP was sending to the RTDS system and what RTDS was recording as an input to the model.

On the other hand there was a need to design a circuitry to interface the output of the RTDS model back to the DSP for closed loop control. Since DSP chips is very sensitive to input and output voltage fluctuations it was decided to design a buffer circuitry in order to protect the DSP from harm while keeping the save level of signal integrity as any distortion could invalidate the closed loop control testing. The combination of the utilizing op-amp in conjunction with using resistors and a capacitor also provided the design with a low pass filter with a cut-off frequency of a few hundred hertz.

As it is evident from figure 4.5 there are four PWM signals. The DSP output signal shows the actual PWM signals outputting from the BJT with 5 volts voltage level. To the right is what is being viewed from the same signals via RTDS. Since at this stage the shape of the signal and the value of phase-shift were of prime importance the time axis values are not shown.
Based on figure 4.6, the circuitry for interfacing the output of the RTDS to the input of the ADC channel of DSP board used a Zener diode in order to make sure that the input signal to the DSP does not exceed a 3.3 V level for safety purposes. The op-amp had a unity gain and R1 was for current limiting and R2 resistor in combination of C1 made a low pass filter.

Figure 4.5: Comparison of DSP output signal and RTDS’ input signal.

Figure 4.6: Low Pass Filter along buffer op-amp for DSP analog to digital input channels.
Finally after the open loop control was successful the circuit was closed to make a real time closed loop control system with the control hardware in the loop provided.

Figure 4.7 is only to show the relationship of the major components of CHIL test. In this figure DSP generates the appropriate PWM signals, sends them to RTDS’ input via BJT bank, then the signal is being received by the model. In this process the model actuates the switches accordingly and simulates the output voltage. Finally the simulated voltage is being read by the DSP by receiving the signal through the RTDS’ output channel and via the buffer circuitry, which was explained earlier.

There are a few designated test points on the RTDS model that was used for troubleshooting and characterizations. The followings are the results of the open and closed loop control in a CHIL approach. The closed and open loop control approaches are compared side by side. It was decided, for open loop a fixed switching frequency that was well within RTDS small signal resolution capabilities and varied the phase shift angles in order to find out what the limitations of the RTDS model were. At the end the frequency also was changed and was
increased from 2kHz to 10kHz and the output voltage and transformer currents were observed. Only the meaningful results were collected.

It is worthy to mention that the PI controller that was implemented yielded to a % 0.5 ripple on the output voltage that is excellent in term of output power quality. [2]

In table 4.1, the open loop results are compared to closed loop results at the same switching frequencies. The output voltage of the RTDS model was scaled so 400 volts would be scaled down to 1 volt. As a rule of thumb the test points that are identified in figure 4.8 are observed in table 4.1. The main and foremost characteristics to identify if the model is behaving well are to observe the currents across the transformer. As a benchmark for the design the current must resemble to what is depicted in figure 4.9.

Figure 4.8: Designated test point location on RTDS model for design verification.
Table 4.1: Open versus closed loop control for CHIL with 30 degree phase shift and 2kHz

<table>
<thead>
<tr>
<th>Parameter Tested</th>
<th>Open Loop Results</th>
<th>Closed Loop Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage of the Model on the scope and scaled to 1 volt.</td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
</tr>
<tr>
<td>Transformer Currents</td>
<td><img src="image3.png" alt="Image" /></td>
<td><img src="image4.png" alt="Image" /></td>
</tr>
<tr>
<td>RTDS Model Output and Input Voltages</td>
<td><img src="image5.png" alt="Image" /></td>
<td><img src="image6.png" alt="Image" /></td>
</tr>
</tbody>
</table>
As it might seem the result for 2kHz switching frequency is very desirable but this frequency is far below the actual values that the current topologies run at. Therefore to find out if the real time simulation can be operated in higher frequencies the frequencies were increased at known steps and for each step the phase shift was increased from 0 degree to its maximum value of 45 degree.

It must be highlighted that the primary benchmark of qualifying the right phase shift value was to observe the transformer currents. In figure 4.9 the transformer current is marked as Ir1. There are two of them in this design. Each current corresponds to a test point identified in figure 4.8.

![Figure 4.9: Ideal Transformer current and its voltages on two sides of the transformer.](image-url)
Table 4.2: Experiment results for qualifying the minimum phase shift.

<table>
<thead>
<tr>
<th>Swt. Freq. (kHz)</th>
<th>Min. ϕ (Deg)</th>
<th>Scope Display Transformer Currents</th>
<th>RTDS Display Vin – Vout</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>3</td>
<td><img src="image1.png" alt="Scope Display" /></td>
<td><img src="image2.png" alt="RTDS Display" /></td>
</tr>
<tr>
<td>2</td>
<td>15</td>
<td><img src="image3.png" alt="Scope Display" /></td>
<td><img src="image4.png" alt="RTDS Display" /></td>
</tr>
</tbody>
</table>

In table 4.2 the results of the closed loop test for various frequencies at various phase-shifts are depicted. The scope display columns show the transformer currents. During research the minimum phase-shift that could result in a reasonable current shape would be recorded. To the right of it is what RDTS model sees as an input and what it outputs. In some cases the output has more ripple than the others. A good design must limit the amount of ripple for efficiency purposes.
As the switching frequency was getting higher we would clearly see that the limits are being pushed on the RTDS capabilities. Therefore the minimum phase-shift we could see that could work with 8kHz switching frequency was 5 degree. For 15 degree of phase-shift for the same frequency the current would start to deteriorate.
The next step from the 5-degree phase-shift was 30 degree of phase-shift. This shows that the control algorithm had a minimum resolution of 25 degree. Please keep in mind that the entire dynamic range of phase shift for the controller to be able to control the output power is 45 degree. For the 10 kHz switching frequency the minimum phase-shift was 40 degree out of 0-45 degree range, which did not produce any meaningful current waveform.
Figure 4.10 illustrates the summary of the CHIL results shown in table 4.2. In addition a pure off-line simulation baseline is presented in this figure to show that CHIL’s results are in accordance with the theoretical results from pure simulations.
CHAPTER FIVE

STUDY OF REAL TIME SIMULATION OF DC-DC CONVERTER ON DSP PLATFORM

As it was mentioned in the earlier chapters there has never been modeling a bi-directional DC-DC converter on a DSP done that would utilize a state-space equation. The proceeding contents will present a case for studying this approach solely because of its code efficiency for real time simulation of high frequency converters.

The idea behind simulating a circuit in real time on a DSP is to derive the entire circuit in mathematical equations and to solve the state equations in order to estimate the next state in the circuit. The state equations would be of a form:

\[
d[x(t)]/dt = A \cdot x(t) + B \cdot u(t) \quad (5.1)
\]

The goal is to identify A and B coefficients. The parameter u(t) is the input to the system and x(t) is the state variable.

To find the A and B coefficients there was a need to derive KVL and KCL for the entire circuit. For this project a voltage fed bi-directional Dual H-Bridge DC-DC converter was chosen.

Figure 5.1: Voltage fed primary referred DHB circuit with all KCL nodes and KVL loops.
In figure 5.1 a short line and a leakage inductor as a result of circuit analysis replace the transformer.

There are a few approaches to solve the state equations with respect the switch status. One is to find all the combinations of the switches and come up with various modes of operations. [5]

Figure 5.2 illustrates a sample of work from [5] that shows different mode of operations as a result of changes in switching modes. The presented circuit here is full bridge converter but it portrays the same concept.

Figure 5.2: Switching modes of operations for a single circuit of full bridge converter.
The disadvantage to this approach is that there will be many operations mode to analyze in real time and calculate the next state of the state variables. This will be computationally intense and time consuming and in some cases won’t lead to a real time performance.

However there is another approach that is discussed in [4]. The working mechanism of a power converter is based upon passive switches. Therefore only switching behavior needs to be modeled. In this proposed simulation approach, power semiconductor switches such as diodes, MOSFET and IGBT are modeled as simple ON/OFF resistance switch (R\textsubscript{ON} = 10 mOhm, R\textsubscript{OFF} = 10 kOhm) with a short dead time presented between switching transitions.

To start the process it was needed to derive the KVL and KCL equations in order to build the equations 5.2 and 5.3. From one circuit topology once can obtain many KVL and KCL variation but only one equation will lead to a right R matrix as you can see the R matrix must be an square matrix with no duplicated rows and columns as R\textsubscript{inv} which the inverse of R must exist.

\[
S(t) = R \cdot N(t) \quad (5.2)
\]

\[
N(t) = R\text{\textsuperscript{-1}} \cdot S(t) \quad (5.3)
\]

After various attempts that are illustrated in the following figures the right R matrix was constructed. The R matrix constructed with duplicated equation would end in infinite determinant. There were various circuit topologies was used but it seemed the R matrix didn’t like the shorted connection between the four capacitors. As a result the short circuit with a small inductor that produced a good R matrix was replaced but caused an unstable output. Please note figure 5.3.

At the end the short was replaced with a very small resistor. The observations about the problem caused by the short circuit can be explained as, since the model is a DC model, the short cannot create a voltage drop therefore two node designators could be used for KCL equations causing to misalignment in the state equation to R matrix but in the actual system the dynamics of the switches create a voltage drop hence it had to be represented by two nodes. Therefore by applying a resistor instead of the short circuit it resulted in an R matrix that had a determinant and also could represent the actual circuit with correct current directions, voltage polarities, number of nodes, and loops. Please note figure 5.4. [7]
Figure 5.3: Attempts to find the right number of KVL and KCL equations.
As a result of applying KVL and KCL the following equations were composed:

\[ N1: 0 = i_{R1} + i_{C1} - i_{in} \]
\[ N2: 0 = i_{R3} + i_{RL} - i_{C3} \]
\[ N3: i_L = i_{R1} - i_{R2} \]
\[ N4: i_L = -i_{R3} + i_{R4} \]
\[ N5: 0 = i_{R4} - i_{c4} + i_{RL} \]
\[ N6: 0 = i_{C1} - i_{C3} - i_{Cc} \]
\[ N7: 0 = i_{C2} - i_{c4} - i_{Cc} \]
\[ L1: V_{in} = R_1i_{R1} + R_2i_{R2} \]
\[ L2: V_{C1} + V_{C3} = R_1i_{R1} + R_4i_{R4} - R_Li_{RL} + V_L \]
\[ L3: V_{C2} + V_{C4} = R_2i_{R2} - R_4i_{R4} - V_L \]
\[ L4: V_{C1} + V_{C2} + V_{C3} + V_{C4} = R_1i_{R1} + R_2i_{R2} - R_3i_{R3} - R_4i_{R4} \]
\[ L5: V_{C1} + V_{C2} = R_1i_{R1} + R_2i_{R2} - R_{Cc}i_{Cc} \]

The state equation is consistent of the following storage variables in the circuit that are all the capacitor voltages and inductor current: [7]

\[ x(t) = \begin{bmatrix} i_L & V_{C1} & V_{C2} & V_{C3} & V_{C4} \end{bmatrix}^T \]
The R matrix that is needed from equation 5.2 is constructed by reorganizing KVL and KCL equations:

\[
R = \begin{bmatrix}
1 & 0 & 0 & 0 & -1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 & 0 \\
1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & -1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & -1 & 0 & 0 & -1 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & -1 & 0 & -1 \\
R_1 & R_2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
R_1 & 0 & 0 & R_4 & 0 & -R_L & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & R_2 & 0 & -R_4 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\
R_1 & R_2 & -R_3 & -R_4 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
R_1 & R_2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -R_{cc}
\end{bmatrix}
\]

The R1 to R4 resistors are the switches that in any state change will be evaluated according to the switching pattern. Therefore any change in R1-R4 values as a result of switching pattern will lead to a change in R matrix hence the inverse of R must be recalculated.

Consequently the S and N matrices were extracted from the same KVL/KCL equations:

\[
S = \begin{bmatrix}
0 \\
0 \\
i_L \\
i_L \\
0 \\
0 \\
V_m \\
V_{C_1} + V_{C_3} \\
V_{C_2} + V_{C_4} \\
V_{C_1} + V_{C_2} + V_{C_4} \\
V_{C_1} + V_{C_2}
\end{bmatrix}
\quad
N = \begin{bmatrix}
i_{R_1} \\
i_{R_2} \\
i_{R_3} \\
i_{R_4} \\
i_m \\
i_{C_1} \\
i_{C_2} \\
i_{C_3} \\
i_{C_4} \\
V_L \\
i_{C_0}
\end{bmatrix}
\]

After the main matrices were constructed the KVL/KCL equations were derived utilizing equations 5.2 and 5.3 and R, S, and N matrices. Please note figure 5.5, Matlab's screenshot of the constructed KVL and KCL equations:
Figure 5.5: Shows screen capture of Matlab KVL and KCL equations for S and F matrices.

\[
F = \\
\begin{align*}
0 \\
0 \\
iL \\
iL \\
0 \\
0 \\
0 \\
Vin \\
VC1 + VC3 \\
VC2 + VC4 \\
VC1 + VC2 + VC3 + VC4 \\
VC1 + VC2 \\
\end{align*}
\]

\[
S = \\
\begin{align*}
iC1 + iR1 - iin \\
iR3 - iC3 + iRL \\
iR1 - iR2 \\
iR4 - iR3 \\
iR4 - iC4 + iRL \\
iC1 - iC3 - icc \\
iC2 - iC4 - icc \\
R1*iR1 + R2*iR2 \\
VL + R1*iR1 + R4*iR4 - RL*iRL \\
R2*iR2 - VL - R4*iR4 \\
R1*iR1 + R2*iR2 - R3*iR3 - R4*iR4 \\
R1*iR1 + R2*iR2 - Rcc*icc \\
\end{align*}
\]
On the other hand the state equations have become:

\[
\frac{d}{dt} x(t) = \begin{bmatrix}
1/C_1 & 0 & 0 & 0 & 0 \\
0 & 1/C_2 & 0 & 0 & 0 \\
0 & 0 & 1/C_3 & 0 & 0 \\
0 & 0 & 0 & 1/C_4 & 0 \\
0 & 0 & 0 & 0 & 1/L
\end{bmatrix} \begin{bmatrix}
i_{C_1} \\
i_{C_2} \\
i_{C_3} \\
i_{C_4} \\
V_L
\end{bmatrix}
\]

According to the reference [4], there are a few utility equations before calculating the A and B values in equation 5.1.

\[F(t) = K_x \cdot x(t) + K_u \cdot u(t) \quad (5.4)\]

\[G(t) = (R_{inv}.K_x)x(t)+(R_{inv}.K_u)u(t) \quad (5.5)\]

The \(K_x\) and \(K_u\) constructed somehow that would lead to \(S(t)\) and \(G(t)\).

\[
K(x) = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
1 & 0 & 1 & 0 & 0 \\
0 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 1 & 0 \\
1 & 1 & 0 & 0 & 0
\end{bmatrix}
\]

\[K(u) = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0
\end{bmatrix}^T\]

\(R_a\) is a special matrix that is calculated with the help of Matlab as it was instructed by reference [4]:

\[R_a=[ \text{inv\_R(7,:)} ; \text{inv\_R(8,:)} ; \text{inv\_R(9,:)} ; \text{inv\_R(10,:)} ; \text{inv\_R(11,:)})]\]

Matrix \(P\) is as follows:

\[
P = \begin{bmatrix}
1/C_1 & 0 & 0 & 0 & 0 \\
0 & 1/C_2 & 0 & 0 & 0 \\
0 & 0 & 1/C_3 & 0 & 0 \\
0 & 0 & 0 & 1/C_4 & 0 \\
0 & 0 & 0 & 0 & 1/L
\end{bmatrix}
\]

Finally \(A\) and \(B\) from equation 5.1 are calculated using Matlab code:

\[A = P.R_a.K_x \quad (5.6)\]

\[B = P.R_a.K_u \quad (5.7)\]
The Matlab code was written based on the following flowchart:

Figure 5.6: Shows the program flow chart

The choice of fixed or variable simulation time step has a major effect on total simulation time duration. Simulation programs designed for all modes case use variable time step. Since the inherent non-linear nature of the power electronic conversion circuit requires extremely small time step in some modes whereas relatively large time steps in other modes. However choosing a small time step does not necessarily yield more accurate results. In the proposed simulation in reference [4] a fixed simulation time step is synchronized with switching instant of switching
power device used in this application example. Switch state of switching power device is checked at each time increment and the state variables switch currents and voltages are calculated. This ensures minimum convergence errors and converter circuits with many active and passive power switching devices can be realized without any complexity from a practical point of view.

As a result a Matlab code was constructed as a pilot program before implementing the algorithm on DSP because troubleshooting in Matlab seemed to be much easier. Matlab built-in differential equation with variable time step was utilized to secure a convergence for the results. The results from the first switching cycle are illustrated in figure 5.7:

<table>
<thead>
<tr>
<th>iL Current from Psim® Simulation</th>
<th>iL Current from Matlab® Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="iL Current from Psim Simulation" /></td>
<td><img src="image2" alt="iL Current from Matlab Simulation" /></td>
</tr>
</tbody>
</table>

**Figure 5.7:** Simulation results from Psim versus Matlab code.

The Matlab simulation was performed with differential solver of Runge-Kutta of fourth order with initial conditions similar to Psim simulation. Psim circuit and Matlab codes have similar parameters except the switches in Psim all have bypass diodes. The time step for ode solver of Matlab is about 10ns and there are 1000 steps for each switching cycle. Although the waveforms in the first simulations are very similar but the maximum current does not match with Psim results.
CONCLUSION AND FUTURE WORK

In addition, after the first switch the current does not converge and it diverges and then oscillates in [-20amp, +20amps] range. Although various ode solvers were tried in which they were using different time steps and signal resolution but the divergence problem yielded in no acceptable results. All the system inputs were checked including the simulated PWM signals, which were driving the gate signals of the switches meaning flipping the resistor R1-R4 values according to the switching pattern and phase-shift of 36 degree. The Matlab model was responsive and showing a dynamic result but the divergence issue was still unresolved. Figure 6.1 illustrates one of the scenarios performed on the model.

Figure 6.1: Shows all the state variables values, iL, VC1-VC4.

Figure 6.2 shows a 36-degree phase-shift, as it is evident on the VC1 and VC2 states.
Figure 6.2: Voltages on capacitor C1 and C3

Figure 6.3: Shows the details of fig. 6.3.
This work is composed of three intertwined projects on studying the DC-DC converter control and simulation in real time. Although converting analog control of a DC-DC converter was not a new concept but it helped the research process to evolve into a good understanding of how a bi-directional DC-DC converter works and most importantly how the control mechanism regulates the output power. In this project the switching pattern was constructed first then the research was moved to implementing the control algorithm on a DSP platform with C language.

Thereafter, the developed control algorithm made the foundation for the second project in which the simulation limitations of the RTDS in a real time simulator was studied. It was concluded that based on RTDS’ objectivity in which it was created to serve large scale power systems with low speed processes, it could not be a suitable match for a high frequency DC-DC converter device. This was a new study and has never been done before and the results were conclusive and presented in the earlier chapters. There was also study if there was a possibility of creating high-speed components via component builder option of the simulator but since this functionality was not available in small time step therefore this option could not be of any help.

Finally the second project led the research to explore the possibility of simulating the entire DC-DC converter hardware on DSP in terms of mathematical equations. Although it did not yield to a definitive answer due to the complexity of the circuit but there are strong promising signs. The divergence problem is most likely developed by the way the circuit is laid out. For the future work the research can be continued in order to develop an specific circuit that resolves the divergence problem as the first switching period has a good shape and the equations developed represents a dynamic circuit that responds to different inputs with different outputs.
REFERENCES

[1] Haiping Xu, DSP-Based Digitally Controlled Bi-directional DC-DC Converter, Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China (2004).


BIOGRAPHICAL SKETCH

(Brian) Mohsen Mirtalebi is an electrical engineer with BSEE from Purdue University. He is pursuing his master’s in electrical engineering at Florida State University. His research background is in power electronics. He has nine years of experience in electronics industry holding job titles ranging from Design Engineer to Manufacturing Engineer and finally Software Engineer.